Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-22 (Cancelled).

Add the following new claims 23-36:

23. (New) A method comprising:

in a parallel processor comprising a controlling processor linked to a remote console system and a plurality of micro engines, each of the micro engines comprising a plurality of executable threads, determining if one of the plurality of treads is executing in a target micro engine;

in response to determining, pausing execution of the threads;

loading hop instructions from a debug library;

storing program counters for the threads;

modifying the program counters of the target micro engine to jump to a start of the hop instructions;

modifying the hop instructions to return to the stored program counters;

copying the hop instructions to an unused segment of micro store in the target micro engine; and

executing the hop instructions.

24. (New) The method of claim 23 further comprising resuming execution of the threads in the target micro engine using the stored program counters.

25. (New) The method of claim 23 wherein pausing comprises receiving a pause command from the remote console system.

26. (New) The method of claim 23 wherein the hop instructions are selected by a user through the remote console system.

27. (New) The method of claim 23 wherein the hop instructions control a start and a stop of selected bus ports with each hop.

27. (New) The method of claim 23 wherein the hop instructions control a start and a stop of selected bus ports with each hop.

28. (New) The method of claim 23 further comprising:

modifying the program counters of the plurality of micro engines to jump to a start of the hop instructions;

modifying the hop instructions to return to the stored program counters;

copying the hop instructions to an unused segment of micro store in the micro engines; and

executing the hop instructions in the micro engines in unison.

29. (New) The method of claim 28 further comprising resuming execution of the threads in the plurality of micro engines using the stored program counters.

30. (New) A processor that can execute multiple contexts that comprises:

a register stack;

a program counter for each executing context;

an arithmetic logic unit coupled to the register stack and a program control store that stores a command that causes the processor to:

determine if one of the multiple contexts is executing in a target micro engine;

in response to determining, pause execution of the multiple contexts;

load hop instructions from a debug library;

store program counters for the multiple contexts;

modify the program counters of the target micro engine to jump to a start of the hop instructions;

modify the hop instructions to return to the stored program counters;

copy the hop instructions to an unused segment of a micro store in the target micro engine; and

execute the hop instructions.

31. (New) The processor of claim 30 wherein the command further causes the processor to:

resume execution of the contexts in the target micro engine using the stored program counters.

32. (New) The processor of claim 30 wherein pausing comprises receiving a pause command from a remote console system.

33. (New) The processor of claim 32 wherein the hop instructions are selected by a user through the remote console system.

34. (New) The processor of claim 30 wherein the hop instructions control a start and a stop of selected bus ports with each hop.

35. (New) The processor of claim 30 wherein the command further causes the processor to:

modify the program counters of the plurality of micro engines to jump to a start of the hop instructions;

modify the hop instructions to return to the stored program counters;

copy the hop instructions to an unused segment of micro store in the micro engines; and

execute the hop instructions in the micro engines in unison.

36. (New) The processor of claim 35 wherein the command further causes the processor to:

resume execution of the threads in the plurality of micro engines using the stored program counters.